What is claimed is:

1. A semiconductor integrated circuit device comprising:

a substrate;

a first conductivity type of semiconductor layers arranged above said substrate as being insulated from said substrate and insulated from each other;

cell transistors formed on the respective semiconductor layers, each of which has a second conductivity type of source, drain layers and a gate electrode to store data in a channel body thereof corresponding to an accumulation state of majority carriers; and

the first conductivity type of emitter layers formed in the respective semiconductor layers to be contacted to the respective drain layers of said cell transistors so as to constitute PN junctions therebetween, the emitter layers serving for injecting majority carriers into the respective channel bodies of said cell transistors.

2. The semiconductor integrated circuit device according to claim 1, wherein

memory cells, each of which is formed of said cell transistor and the corresponding emitter layer, are arranged in a matrix manner to constitute a cell array, and wherein

said cell array comprises word lines each commonly connected to the gate electrodes of said cell transistors arranged in a first direction of the matrix, bit lines each commonly connected to the drain layers of said cell transistors arranged in a second direction of the matrix, source lines each commonly connected to the source layers of said cell transistors arranged in the first direction, and emitter lines each commonly connected to the emitter layers arranged in the first direction.

3. The semiconductor integrated circuit device according to claim 2, wherein

said memory cells are formed on the respective semiconductor layers.

4. The semiconductor integrated circuit device according

to claim 2, wherein

adjacent two memory cells are formed on each of said semiconductor layers arranged in the second direction with a shared source layer.

5. The semiconductor integrated circuit device according to claim 2, wherein

each said cell transistor stores one of first and second data states, the first data state being defined as a state that holds excessive majority carriers in the channel body, the second data state being defined as a state that holds less majority carriers than the first data state.

6. The semiconductor integrated circuit device according to claim 5, wherein

the first data state of said cell transistor is written by applying a forward bias between the drain layer and the corresponding emitter layer so as to inject majority carriers from the emitter layer into the channel body, and wherein

the second data state of said cell transistor is written by releasing the majority carries held in the channel body toward the drain layer.

7. The semiconductor integrated circuit device according to claim 5, wherein

the first data state is written under the condition of $VBLS+V1 \leqq VELS$, $VELS \leqq VBLU+V0$ and $VELU \leqq VBLS+V0$, where VBLS is a selected bit line voltage; VBLU an unselected bit line voltage; VELS a selected emitter line voltage; VELU an unselected emitter line voltage; V1 a voltage necessary for forward-biasing the PN junction between the drain and emitter layers; and V0 a voltage insufficient for forward-biasing the PN junction between the drain and emitter layers.

8. The semiconductor integrated circuit device according to claim 7, wherein

during the first data state is written, a voltage is applied to the entire word lines to turn off said cell transistors.

9. The semiconductor integrated circuit device according

to claim 7, wherein

during the first data state is written, a voltage is applied to unselected word lines to turn off said cell transistors, and another voltage is applied to a selected word lines as being higher than that applied to the unselected word lines.

10. The semiconductor integrated circuit device according to claim 7, wherein

data writing operations of the first and second data states for plural memory cells with a shared word line are performed at different timings from each other.

11. The semiconductor integrated circuit device according to claim 5, further comprising:

current sensing type sense amplifiers smaller in number than said memory cells arranged in the first direction of said cell array; and

bit line selectors for connecting selected bit lines in said cell array to the corresponding sense amplifiers.

12. The semiconductor integrated circuit device according to claim 11, wherein

said device has a data write mode with first and second steps, the first step serving for writing the first data state into the entire memory cells selected by said bit line selectors, the second step serving for writing the second data state into memory cells into which the second data state is to be written.

13. The semiconductor integrated circuit device according to claim 11, wherein

said device has a data write mode with first and second steps, the first step serving for writing the second data state into the entire memory cells selected by said bit line selectors, the second step serving for writing the first data state into memory cells into which the first data state is to be written.

14. The semiconductor integrated circuit device according to claim 11, wherein

said device has a data write mode with first and second steps, the first step serving for writing the first data state into some ones in memory cells selected by said bit line selectors, into which the first data is to be written, the second step serving for writing the second data state into the others in memory cells selected by said bit line selectors, into which the second data state is to be written.

15. The semiconductor integrated circuit device according to claim 11, wherein

said device has a data write mode with first and second steps, the first step serving for writing the second data state into some ones in memory cells selected by said bit line selectors, into which the second data is to be written, the second step serving for writing the first data state into the others in memory cells selected by said bit line selectors, into which the first data state is to be written.

16. The semiconductor integrated circuit device according to claim 11, wherein

said device has a data write mode that data write operations of the first and second data states are simultaneously performed for the entire memory cells selected by said bit line selectors.

17. A semiconductor integrated circuit device comprising:

a substrate;

a first conductivity type of semiconductor layers arranged above said substrate as being insulated from said substrate and from each other;

cell transistors formed on the respective semiconductor layers, each of which has a second conductivity type of source, drain layers and a gate electrode to store data in a channel body thereof corresponding to an accumulation state of majority carriers; and

bipolar transistors each having the first conductivity type of emitter layer formed to be contacted to each the drain layer, and having base and collector layers defined by the

drain layer and channel body of each said cell transistor respectively, wherein

each said cell transistor stores one of first and second data states, the first data state being defined as a state that holds excessive majority carriers in the channel body thereof, the second data state being defined as a state that holds less majority carriers than the first data state.

18. The semiconductor integrated circuit device according to claim 17, wherein

the first data state of said cell transistor is written by turning on the corresponding bipolar transistor to inject majority carriers from the emitter layer into the channel body via the drain layer, and wherein

the second data state of said cell transistor is written by releasing the majority carries held in the channel body toward the drain layer while letting the corresponding bipolar transistor be off.